

## Product Features

- Compliant with IEEE Std 802.3-2005  
10G Ethernet 10GBase-ZR/ZW
- Electrical interface specifications per SFF-8431
- Management interface specifications per SFF-8431 and SFF-8472
- SFP+ MSA package with duplex LC connector
- Cooled EML Laser
- Dual CDR from 9.95 to 11.3Gb/s bi-directional data links
- Single +3.3V power supply
- Class 1 laser safety certified
- Operating temperature: -40°C to +85°C
- Up to 80km on 9/125µm SMF
- RoHS Compliant



## Applications

- 10G Ethernet 10GBASE-ZR/ZW
- 80km 10G Fiber Channel
- 80km 10Gb/s DWDM SONET/SDH

## Descriptions

LX42xxIDH SFP+ transceivers, according to Enhanced 8.5 and 10 Gigabit Small Form Factor Pluggable “SFP+” Multi-Sourcing Agreement (MSA) SFF-8431 and SFF-8472, revision 10.4, are high performance and cost effective transceivers. They meet the requirements for 10Gb/s DWDM SONET/SDH ITU-T G.959.1 PIL1-2D2, 80km DWDM 10G Ethernet 10GBase-ZR/ZW, and 80km 10G Fiber Channel.

LX42xxIDH are compliant with RoHS.

## Ordering Information

**Table 1. Ordering Information**

Part Number	Transmitter	Output Power	Receiver	Sensitivity	Reach	Temp	DDM	RoHS
LX42xxIDH	DWDM EML	0 ~ +4dBm	APD	< -23dBm	80km	-40 ~ 85°C	Available	Compliant

**Notes:** See Table 2 – Wavelength Guide for “xx” value.

**Table 2. Wavelength Guide for “xx” value (100GHz ITU-T channel)**

Channel #	Product Part Number	Frequency (THz)	Center Wavelength (nm)
17	LX4217IDH	191.7	1563.86
18	LX4218IDH	191.8	1563.05
19	LX4219IDH	191.9	1562.23
20	LX4220IDH	192.0	1561.42



**LX42xxIDH**  
**10GEthernet 80km DWDM SFP+ Transceiver**  
**10Gb DWDM SDH / 10GBASE-ZR**

21	LX4221IDH	192.1	1560.61
22	LX4222IDH	192.2	1559.79
23	LX4223IDH	192.3	1558.98
24	LX4224IDH	192.4	1558.17
25	LX4225IDH	192.5	1557.36
26	LX4226IDH	192.6	1556.55
27	LX4227IDH	192.7	1555.75
28	LX4228IDH	192.8	1554.94
29	LX4229IDH	192.9	1554.13
30	LX4230IDH	193.0	1553.33
31	LX4231IDH	193.1	1552.52
32	LX4232IDH	193.2	1551.72
33	LX4233IDH	193.3	1550.92
34	LX4234IDH	193.4	1550.12
35	LX4235IDH	193.5	1549.32
36	LX4236IDH	193.6	1548.51
37	LX4237IDH	193.7	1547.72
38	LX4238IDH	193.8	1546.92
39	LX4239IDH	193.9	1546.12
40	LX4240IDH	194.0	1545.32
41	LX4241IDH	194.1	1544.53
42	LX4242IDH	194.2	1543.73
43	LX4243IDH	194.3	1542.94
44	LX4244IDH	194.4	1542.14
45	LX4245IDH	194.5	1541.35
46	LX4246IDH	194.6	1540.56
47	LX4247IDH	194.7	1539.77
48	LX4248IDH	194.8	1538.98
49	LX4249IDH	194.9	1538.19
50	LX4250IDH	195.0	1537.40
51	LX4251IDH	195.1	1536.61
52	LX4252IDH	195.2	1535.82
53	LX4253IDH	195.3	1535.04
54	LX4254IDH	195.4	1534.25
55	LX4255IDH	195.5	1533.47
56	LX4256IDH	195.6	1532.68
57	LX4257IDH	195.7	1531.90

58	LX4258IDH	195.8	1531.12
59	LX4259IDH	195.9	1530.33
60	LX4260IDH	196.0	1529.55
61	LX4261IDH	196.1	1528.77

## Pin Description

**Table 2. Pin Description**

Pin	Name	Function/Description	Notes
1	VeeT	Transmitter Ground	1
2	TX_Fault	Transmitter Fault (LVTTTL-O) - High indicates a fault condition	2
3	TX_Disable	Transmitter Disable (LVTTTL-I) – High or open disables the transmitter	3
4	SDA	Two wire serial interface Data Line (LVCMOS-I/O) (MOD-DEF2)	4
5	SCL	Two wire serial interface Clock Line (LVCMOS-I/O) (MOD-DEF1)	4
6	MOD_ABS	Module Absent (Output), connected to VeeT or VeeR in the module	5
7	RS0	Rate Select 0 – Not used, Presents high input impedance	-
8	RX_LOS	Receiver Loss of Signal (LVTTTL-O)	2
9	RS1	Rate Select 1 – Not used, Presents high input impedance	-
10	VeeR	Receiver Ground	1
11	VeeR	Receiver Ground	1
12	RD-	Inverse Received Data out (CML-O)	-
13	RD+	Received Data out (CML-O)	-
14	VeeR	Receiver Ground	-
15	VccR	Receiver Power - +3.3V	-
16	VccT	Transmitter Power - +3.3 V	-
17	VeeT	Transmitter Ground	1
18	TD+	Transmitter Data In (CML-I)	-
19	TD-	Inverse Transmitter Data In (CML-I)	-
20	VeeT	Transmitter Ground	1

**Notes:**

1. The module signal grounds are isolated from the module case.
2. This is an open collector/drain output that on the host board requires a 4.7K $\Omega$  to 10K $\Omega$  pull-up resistor to VccHost.
3. This input is internally biased high with a 4.7K $\Omega$  to 10K $\Omega$  pull-up resistor to VccT.
4. Two-Wire Serial interface clock and data lines require an external pull-up resistor dependent on the capacitance load.
5. This is a ground return that on the host board requires a 4.7K $\Omega$  to 10K $\Omega$  pull-up resistor to VccHost.

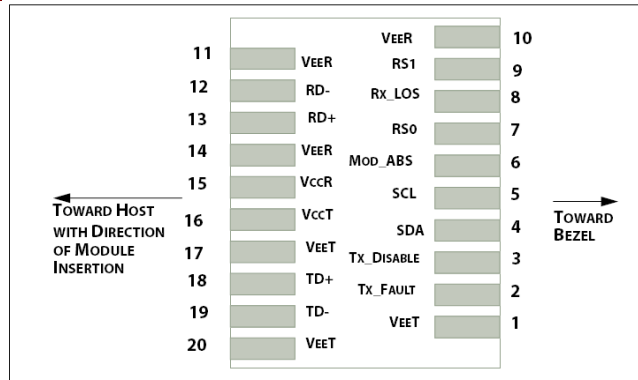


Figure 1. Host PCB SFP+ pad assignment top view

## Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

**Table 3. Absolute Maximum Ratings**

Parameter	Symbol	Minimum	Maximum	Unit
Storage Temperature	T <sub>s</sub>	-40	85	°C
Relative Humidity	RH	5	95	%
Supply Voltage	V <sub>cc</sub>	-0.5	4.0	V

## Recommended Operating Conditions

**Table 4. Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Operating Case Temperature	T <sub>c</sub>	-40	25	85	°C
Supply Voltage	V <sub>cc</sub>	3.135	3.3	3.465	V
Data Rate	-	9.95	-	11.31	Gb/s

## Transceiver Electrical Characteristics

**Table 5. Transceiver Electrical Characteristics**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Module Supply Current	I <sub>cc</sub>	-	400	660	mA	-
Power Dissipation	P <sub>D</sub>	-	1.3	2.2	W	-
<b>Transmitter</b>						
Input Differential Impedance	Z <sub>IN</sub>	-	100	-	Ω	-

Differential Data Input Swing		$V_{IN, P-P}$	180	-	700	mV <sub>P-P</sub>	-
TX_FAULT	Transmitter Fault	$V_{OH}$	2.0	-	$V_{CCHOST}$	V	-
	Normal Operation	$V_{OL}$	0	-	0.8	V	-
TX_DISABLE	Transmitter Disable	$V_{IH}$	2.0	-	$V_{CCHOST}$	V	-
	Transmitter Enable	$V_{IL}$	0	-	0.8	V	-
<b>Receiver</b>							
Output Differential Impedance		$Z_O$	-	100	-	$\Omega$	-
Differential Data Output Swing		$V_{OUT, P-P}$	300	-	850	mV <sub>P-P</sub>	1
Data Output Rise Time, Fall Time		$t_r, t_f$	28	-	-	ps	2
RX_LOS	Loss of signal (LOS)	$V_{OH}$	2.0	-	$V_{CCHOST}$	V	3
	Normal Operation	$V_{OL}$	0	-	0.8	V	3

**Notes:**

1. Internally AC coupled, but requires a external 100 $\Omega$  differential load termination.
2. 20–80%.
3. LOS is an open collector output. Should be pulled up with 4.7k $\Omega$  on the host board.

## Transmitter Optical Characteristics

**Table 6. Transmitter Optical Characteristics**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Launch Optical Power	$P_o$	0	-	+4.0	dBm	1
Center Wavelength Range	$\lambda_c$	1528.77	-	1563.86	nm	-
Center Wavelength Spacing	-	-	100	-	GHz	
Center Wavelength Tolerance	$\Delta\lambda_c$	-100	-	100	pm	
Extinction Ratio	EX	9.0	-	-	dB	2
Side Mode Suppression Ratio	SMSR	30	-	-	dB	-
Transmitter and Dispersion Penalty	TDP	-	-	3.0	dB	-
Relative Intensity Noise	RIN			-128	dB/Hz	
Optical Return Loss Tolerance	ORLT	-	-	21	dB	-
Pout @TX-Disable Asserted	$P_{off}$	-	-	-30	dBm	1
Eye Diagram						ITU-T G.691 SDH STM-64 L-64.2 compatible

**Notes:**

1. The optical power is launched into 9/125 $\mu$ m SMF.
2. Measured with a PRBS 2<sup>31</sup>-1 test pattern @10.3Gbps.

## Receiver Optical Characteristics

**Table 7. Receiver Optical Characteristics**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Center Wavelength	$\lambda_c$	1260	-	1610	nm	-
Receiver Sensitivity ( $P_{avg}@9.95\text{Gb/s}$ )	S	-	-	-24	dBm	1
Receiver Sensitivity ( $P_{avg}@11.1\text{Gb/s}$ )	S			-22	dBm	1
Receiver Overload ( $P_{avg}$ )	$P_{OL}$	-7.0	-	-	dBm	2
Optical Return Loss	ORL	26	-	-	dB	-
LOS De-Assert	$LOS_D$	-	-	-25	dBm	-
LOS Assert	$LOS_A$	-37	-	-	dBm	-
LOS Hysteresis	-	0.5	-	-	dB	-

**Notes:**

1. Measured with PRBS  $2^{31}-1$  test pattern,  $BER < 10^{-12}$ .
2. Comply with IEEE 802.3-2005.

## Recommended Host Board Power Supply Filter Network

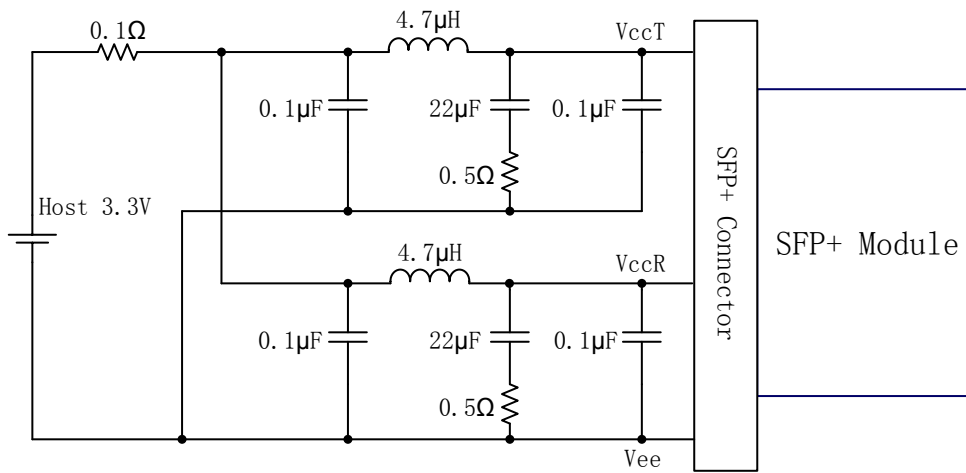


Figure 2. Recommended Host Board Power Supply Filter Network

## Recommended Application Interface Block Diagram

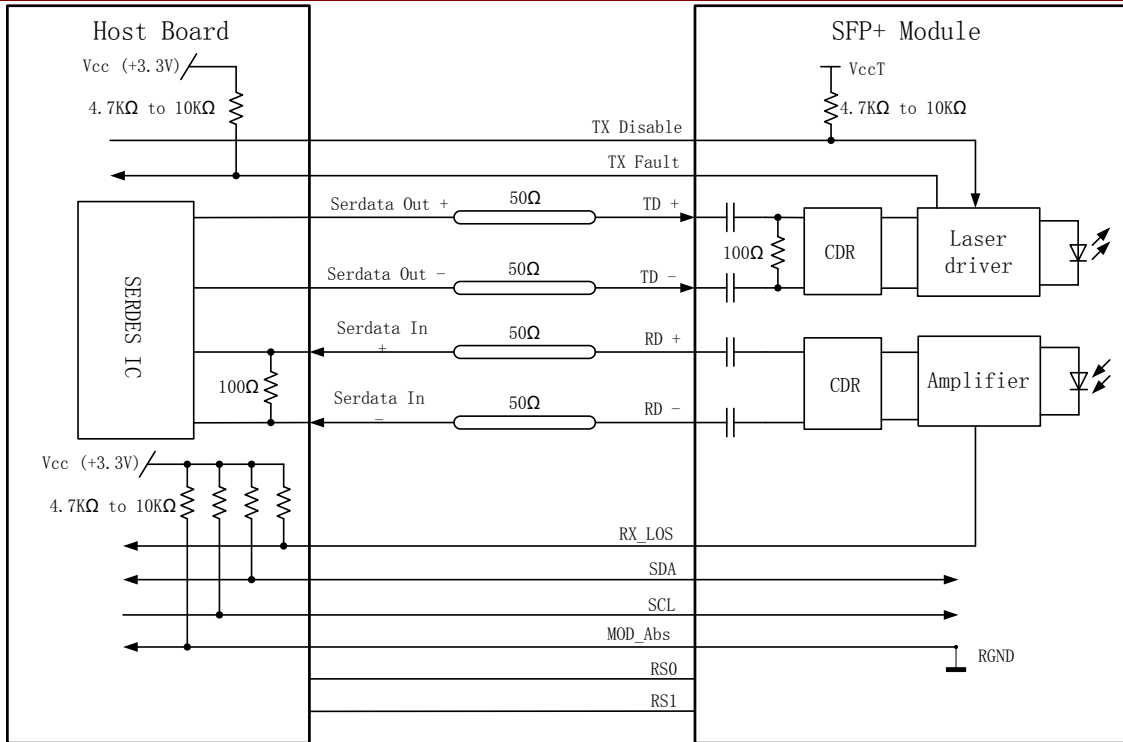


Figure 3. Recommended Application Interface Block Diagram

## Mechanical specifications

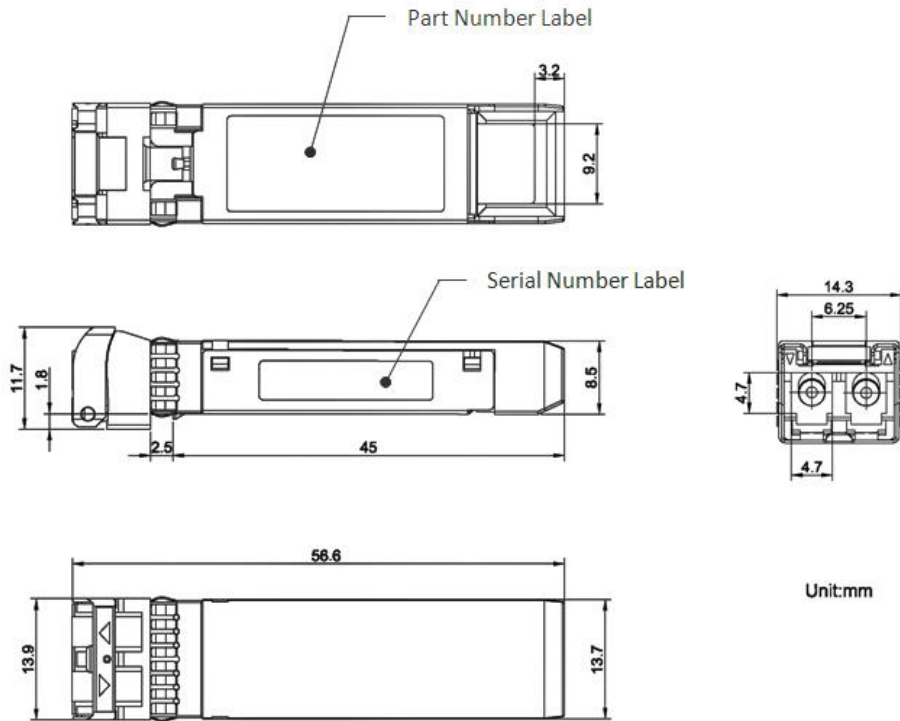


Figure 4. Outline Drawing

## PCB layout recommendation



- Notes:
1. Datum and basic dimensions established by customer
  2. Pads and vias are chassis ground, 11 places
  3. Thru holes, plating optional

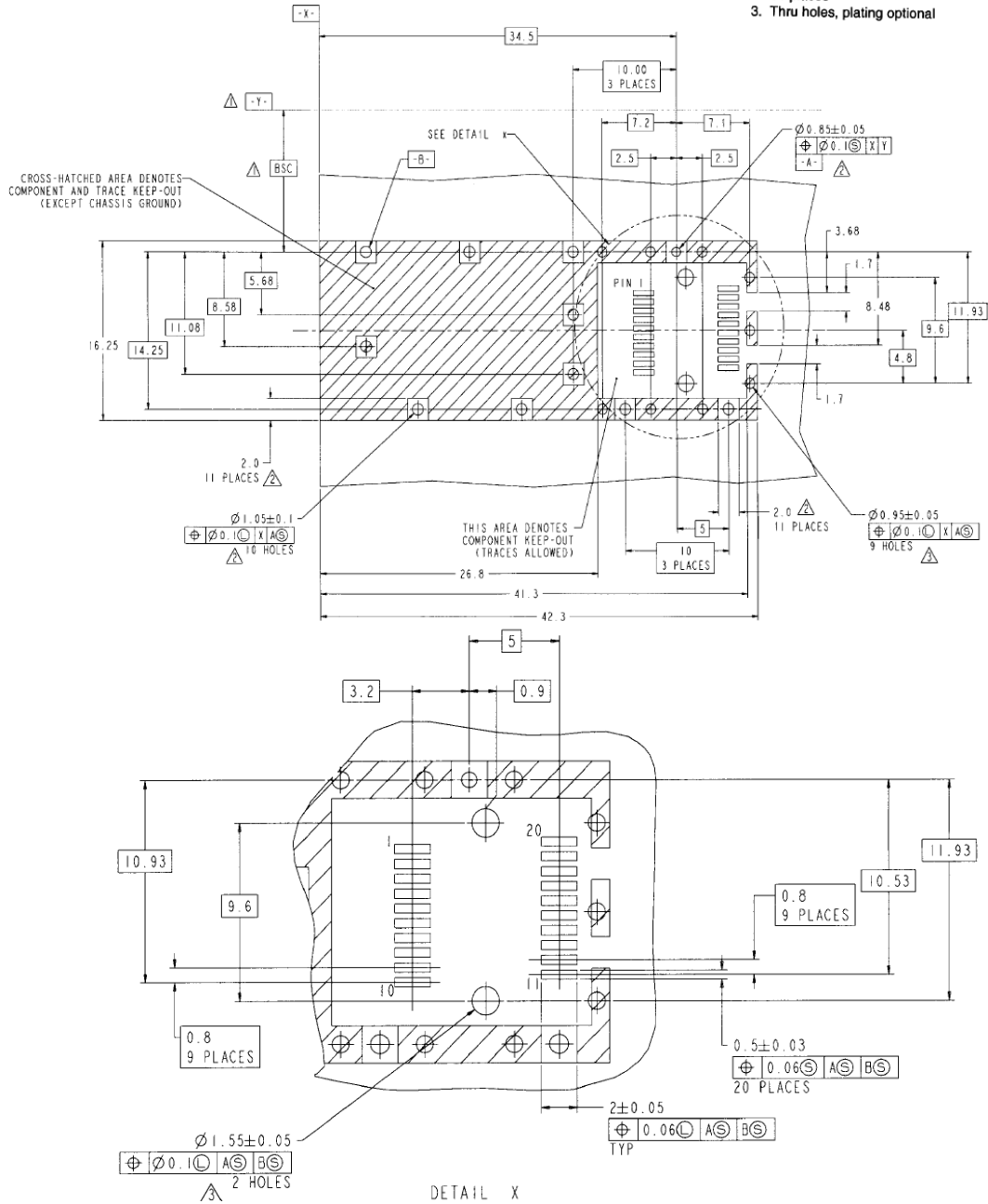


Figure 5. PCB layout recommendation

**For More Information**

**Linktel Technologies Co., Ltd**



**LX42xxIDH**  
**10GEthernet 80km DWDM SFP+ Transceiver**  
**10Gb DWDM SDH / 10GBASE-ZR**

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